WHAT IS CLAIMED:

1. An integrated circuit device comprising:

a conductive contact in a hole in an interlevel dielectric layer;

a first spacer having a first dielectric constant on a side wall of the conductive contact; and

a second spacer having a second dielectric constant that is less than the first dielectric constant located between the first spacer and the side wall of the conductive contact.

2. An integrated circuit device according to Claim 1 wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide.

3. An integrated circuit device of Claim 1, wherein the thickness of the first spacer is in a range between about 10 Å and about 300 Å.

4. An integrated circuit device according to Claim 1 wherein the thickness of the second spacer is in a range between about 10 Å and about 200 Å.

5. An integrated circuit device according to Claim 1 further comprising:

a conductive line in the interlevel dielectric layer adjacent the first spacer opposite the conductive contact.

6. An integrated circuit device according to Claim 1 further comprising:

a contact pad in a substrate, wherein the conductive plug contacts the contact pad.

7. An integrated circuit device according to Claim 6 wherein the second spacer extends along the side wall to contact the contact pad; and

wherein the first spacer does not contact the spaced isolated from the contact pad.

8. An integrated circuit device comprising:

a substrate;

a first interlevel dielectric layer which is formed on the substrate, wherein contact holes are formed in the first interlevel dielectric layer;

first contact spacers which are formed along the side walls of the first interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers which are formed of silicon nitride and formed on the first spacer; and

contact plugs which are formed between the second contact spacers.

9. The integrated circuit device of claim 8, wherein between the substrate and the first interlevel dielectric layer, further comprising:

a second interlevel dielectric layer which is formed on the substrate; and

contact pads which are formed in the second interlevel dielectric layer and electrically connected to the contact plugs.

10. An integrated circuit device comprising:

an integrated circuit substrate in which source/drain regions are formed;

a first interlevel dielectric layer which is formed on the integrated circuit substrate;

gate line patterns which are formed in the first interlevel dielectric layer;

contact pads which are present between adjacent gate line patterns in the first interlevel dielectric layer and electrically connected to the source/drain regions;

a second interlevel dielectric layer which is formed on the first interlevel dielectric layer, wherein contact holes, through which the contact pads are exposed, are formed in the second interlevel dielectric layer;

first contact spacers which are formed along the side walls of the second interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers which are formed of silicon nitride and formed on the first contact spacers; and

contact plugs which are present in the contact holes between the second contact spacers.

11. The integrated circuit device of claim 10, wherein the second interlevel dielectric layer further comprises:

bit line contact plugs which are electrically connected to some of the contact pads; and

bit line patterns which are formed on the bit line contact plugs and electrically connected to the bit line contact plugs,

wherein the other contact pads, which are not electrically connected to the bit line contact plugs, are exposed through the contact holes.

12. A method of fabricating an integrated circuit device, comprising:

forming a first spacer having a first dielectric constant on a side wall of an interlevel dielectric layer that defines a contact hole in the interlevel dielectric layer;

forming a second spacer having a second dielectric constant that is greater than the first dielectric constant on the first spacer; and

forming a conductive contact in the hole.

13. A method according to Claim 12 further comprising:

removing a portion of the second spacer from a bottom of the hole to expose the first spacer, wherein a remnant portion of the first spacer remain at the bottom; and

removing the remnant portion and the first spacer from the bottom to expose an underlying contact pad.

14. A method according to Claim 12 wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide.

15. A method according to Claim 12 further comprising:

forming a conductive line in the interlevel dielectric layer adjacent the first spacer opposite the second spacer.

16. A method of fabricating an integrated circuit device, comprising:

forming a first interlevel dielectric layer on a substrate;

forming contact holes in the first interlevel dielectric layer;

forming first contact spacers along the side walls of the first interlevel dielectric layer which is exposed through the contact holes, the first contact spacers being formed of silicon oxide;

forming second contact spacers on the first contact spacers, using silicon nitride; and

forming contact plugs by filling a conductive material in the contact holes between the second contact spacers.

17. The method of claim 16, wherein the contact pads are formed of polysilicon or metal.

18. The method of claim 16, wherein the formation of the first and second contact spacers comprises:

forming a silicon oxide layer on the first interlevel dielectric layer conformally, the first interlevel dielectric layer including the contact holes;

forming a silicon nitride layer on the silicon oxide layer;

forming second contact spacers by etching the silicon nitride layer; and

forming first contact spacers by etching the silicon oxide layer.

19. The method of claim 18, wherein the formation of the silicon oxide layer is performed using atomic layer deposition (ALD) or chemical vapor deposition (CVD).

20. The method of claim 18, wherein the formation of the silicon nitride layer is performed using ALD or CVD.

21. The method of claim 18, after the formation of the first contact spacers, further comprising a process of eliminating remnant silicon nitride.

22. The method of claim 16, before the formation of the contact plugs further comprising a precleaning process.

23. The method of claim 22, wherein the precleaning process is performed using a chemical composition containing an agent that has excellent etching characteristics with respect to silicon oxide.

24. The method of claim 16, wherein the formation of the contact holes is performed using a photo mask of hole type or line type.

25. A method of fabricating an integrated circuit device, comprising:

forming gate line patterns on an integrated circuit substrate;

forming a first interlevel dielectric layer on the integrated circuit substrate and the gate line patterns;

forming contact pads on the first interlevel dielectric layer, the contact pads being electrically connected to a particular region of the integrated circuit substrate;

forming a second interlevel dielectric layer on the resultant structure;

forming contact holes on the second interlevel dielectric layer to expose the contact pads;

forming first contact spacers along the side walls of the second interlevel dielectric layer which is exposed through the contact holes, the first contact spacers being formed of silicon oxide;

forming second contact spacers on the first contact spacers, the second contact spacers being formed of silicon nitride; and

forming contact plugs by filling a conductive material in the contact holes between the second contact spacers.

26. The method of claim 25, after the formation of the second interlevel dielectric layer, further comprising:

forming bit line contact plugs and bit line patterns on the second interlevel dielectric layer, the bit line contact plugs being electrically connected to some of the contact pads; and

forming a third interlevel dielectric layer on the resultant structure,

wherein the contact holes are formed on the second and third interlevel dielectric layers so as to expose the other contact pads which are not connected to the bit line contact plugs.

27. The method of claim 26, wherein the formation of the first and second contact spacers comprise:

forming a silicon oxide layer on the first interlevel dielectric layer to match the first interlevel dielectric layer, the first interlevel dielectric layer including the contact holes;

forming a silicon nitride layer on the silicon oxide layer;

forming second contact spacers by etching the silicon nitride layer; and

forming first contact spacers by etching the silicon oxide layer.